UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,684	02/27/2002	Tomonari Yamamoto	020254	1544

23850 7590 10/06/2003

ARMSTRONG, KRATZ, QUINTOS, HANSON & BROOKS, LLP
1725 K STREET, NW
SUITE 1000
WASHINGTON, DC 20006

EXAMINER	
ERDEM, FAZLI	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/083,684	YAMAMOTO, TOMONARI	
	Examiner	Art Unit	
	Fazli Erdem	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 February 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13,15-18,20-23 and 25-30* is/are rejected.

7)☒ Claim(s) *14,19 and 24* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Allowable Subject Matter

1. Claims 14, 19, and 24 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 13, 15, and 16rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. (5,736,438) in view of Yamazaki et al. (5,824,574) further in view of Kawaguchi (6,245,622).

Regarding Claims 1, 2, 13, 15, and 16 Nishimura et al. disclose a field effect thin-film transistor and method of manufacturing the same as well as semiconductor device provided with the same where a field effect transistor formed on an insulator includes an active layer and a gate electrode. Gate electrode is formed on a channel region of the active layer with a gate insulating film therebetween. The active layer is formed of a channel region and source/drain regions. The channel region is formed of a monocrystal silicon layer and does not include a grain boundary. The source/drain regions are formed of a polysilicon layer. Nishimura et al. fail to disclose the required method of laser irradiation, and impurity introduction. However, Yamazaki et al. disclose a semiconductor material, a semiconductor device using the same, and a manufacturing

method thereof where the required laser irradiation method is shown. Furthermore, Kawaguchi et al. disclose a method for fabricating semiconductor integrated circuit device including step of forming self-aligned metal silicide film where the required method of impurity introduction is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required method of laser irradiation and the required method of impurity introduction in Nishimura et al. as taught by Yamazaki et al. and Kawaguchi in order to make a semiconductor device with higher performance.

3. Claims 3-8 rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. (5,736,438) in view of Yamazaki et al. (5,824,574) further in view of Kawaguchi (6,245,622) further in view of Talwar et al. (5,908,307) further in view of Noda et al. (6,432,802).

Regarding Claims 3-8, Nishimura et al. disclose a field effect thin-film transistor and method of manufacturing the same as well as semiconductor device provided with the same where a field effect transistor formed on an insulator includes an active layer and a gate electrode. Gate electrode is formed on a channel region of the active layer with a gate insulating film therebetween. The active layer is formed of a channel region and source/drain regions. The channel region is formed of a monocrystal silicon layer and does not include a grain boundary. The source/drain regions are formed of a polysilicon layer. Nishimura et al. fail to disclose the required method of laser irradiation, impurity introduction, junction/wall fabrication, and shallow/deep junction fabrication. However, Yamazaki et al. disclose a semiconductor material, a semiconductor device using the same, and a manufacturing method thereof where the required

laser irradiation method is shown. Furthermore, Kawaguchi et al. disclose a method for fabricating semiconductor integrated circuit device including step of forming self-aligned metal silicide film where the required method of impurity introduction is disclosed. Talwar et al. disclose a fabrication method for reduced-dimension FET devices where the required method of junction/wall fabrication is disclosed. Noda et al. disclose a method for fabricating semiconductor device where the required method of shallow/deep junction fabrication is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required method of laser irradiation, required method of impurity introduction, junction/wall fabrication, and shallow/deep junction fabrication in Nishimura et al. as taught by Yamazaki et al., and Kawaguchi, Talwar et al, and Noda et al. in order to make a semiconductor device with higher performance.

4. Claims 9-12 rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. (5,736,438) in view of Yamazaki et al. (5,824,574) further in view of Kawaguchi (6,245,622) further in view of Yoshimi et al. (5,698,869).

Regarding Claims 9-12, Nishimura et al. disclose a field effect thin-film transistor and method of manufacturing the same as well as semiconductor device provided with the same where a field effect transistor formed on an insulator includes an active layer and a gate electrode. Gate electrode is formed on a channel region of the active layer with a gate insulating film therebetween. The active layer is formed of a channel region and source/drain regions. The channel region is formed of a monocrystal silicon layer and does not include a grain boundary. The source/drain regions are formed of a polysilicon layer. Nishimura et al. fail to disclose the

required method of laser irradiation, impurity introduction, and junction/wall fabrication. However, Yamazaki et al. disclose a semiconductor material, a semiconductor device using the same, and a manufacturing method thereof where the required laser irradiation method is shown. Furthermore, Kawaguchi et al. disclose a method for fabricating semiconductor integrated circuit device including step of forming self-aligned metal silicide film where the required method of impurity introduction is disclosed. Yoshimi et al. disclose an insulated-gate transistor having narrow-bandgap source where the required junction/wall fabrication is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required method of laser irradiation, therequired method of impurity introduction, and the junction/wall fabrication in Nishimura et al. as taught by Yamazaki et al., Kawaguchi, and Yoshimi et al. in order to make a semiconductor device with higher performance.

5. Claims 18, 20, 21, 22, 23, 25 and 26 rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. (5,736,438) in view of Shimizu et al. (6,017,781) further in view of Nakajima et al. (5,712,191) further in view of Yoshimi et al. (5,698,869) further in view of Noda et al. (6,432,802).

Regarding Claims 18, 20, 21, 22, 23, 25, and 26 Nishimura et al. disclose a field effect thin-film transistor and method of manufacturing the same as well as semiconductor device provided with the same where a field effect transistor formed on an insulator includes an active layer and a gate electrode. Gate electrode is formed on a channel region of the active layer with a gate insulating film therebetween. The active layer is formed of a channel region and

source/drain regions. The channel region is formed of a monocrystal silicon layer and does not include a grain boundary. The source/drain regions are formed of a polysilicon layer. Nishimura et al. fail to disclose the required method of impurity introduction, laser irradiation, junction/wall fabrication, and shallow/deep junction fabrication. However, Shimizu et al. disclose a method of making a thin film transistor where the required method of impurity introduction is disclosed. Furthermore, Nakajima et al. disclose a method for producing semiconductor device where the required laser irradiation is disclosed. Yoshimi et al. disclose an insulated-gate transistor having narrow bandgap source where the required junction/wall fabrication method is disclosed. Noda et al. disclose a method for fabricating semiconductor device where the required shallow/deep junction fabrication is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required method of impurity introduction, laser irradiation, junction/wall fabrication, and shallow/deep junction fabrication in Nishimura et al. as taught by Shimizu, Nakajima et al., Yoshimi et al., and Noda et al. respectively in order to make a semiconductor device with higher performance.

6. Claims 27-30 rejected under 35 U.S.C. 103(a) as being unpatentable over Nishimura et al. (5,736,438) in view of Kawaguchi (6,245,622) further in view of Chong et al. (6,335,253).

Regarding Claims 1, 2, 13, 15, and 16 Nishimura et al. disclose a field effect thin-film transistor and method of manufacturing the same as well as semiconductor device provided with the same where a field effect transistor formed on an insulator includes an active layer and a gate electrode. Gate electrode is formed on a channel region of the active layer with a gate insulating

film therebetween. The active layer is formed of a channel region and source/drain regions. The channel region is formed of a monocrystal silicon layer and does not include a grain boundary. The source/drain regions are formed of a polysilicon layer. Nishimura et al. fail to disclose the required impurity introduction and shallow/deep junction structures. However, Kawaguchi et al. disclose a method for fabricating semiconductor integrated circuit device including step of forming self-aligned metal silicide film where the required impurity introduction is disclosed. Furthermore, Chong et al. disclose a method to form MOS transistors with shallow junctions using laser annealing where the required shallow/deep junction structure is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required impurity introduction and shallow/deep junction structures in Nishimura et al. as taught by Kawaguchi and Chong et al. respectively in order to have a semiconductor device with better performance.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (703) 305-3868. The examiner can normally be reached on M - F 8:00 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

FE